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Influence on LSI Package Wireability of Via Availability and Wiring Track Accessibility

In this paper, experiments are reported which use automatic global and line-packing wiring routines, supplemented by a restricted maze runner, to evaluate the overall influences of several important physical variables upon the wireability of several logic-circuit package types. The logic circuits are contained in subpackages (e.g., modules carrying chips), which are inserted, using pins, into the carrier package in a regular array of holes otherwise available as vias interconnecting the wiring planes. Over a range of connection counts from several hundred to several thousand, it is found that "overflows" (connections not wired by the program) amounting to as much as 10 or 15% of the wires can be substantially reduced in number by careful design. This can be done by using a sufficient number of programmable vias (greater than one per used pin) and by using a track grid ensuring maximum global track accessibility to all pins, or by a combination of both of these tactics in conjunction with suitable wiring algorithms. Some simple theoretical arguments are given which characterize the design problem in the light of the results.

1. Introduction

The problems in wiring together large numbers of logic circuits packaged in digital systems are widely recognized. The advent of large and very large scale integration causes these problems to pervade the package hierarchy all the way down to the chip level. A convenient summary of many of the algorithms developed over a period of years to give computer assistance in solving these problems has been given by Hightower, who has also originated important contributions to automatic wiring [1]. Key insight into the nature of the wiring problem has been given by Donath [2, 3] (Donath's hierarchical theory of logic design gives an upper bound for the variation of the average length of wires resulting from purposeful placement of logic circuits) and by M. Feuer [4]. Donath's work [5] and Feuer's work also predict an experimentally verified *increase* of average wire length with a fractional power of circuit count based upon "Rent's Rule." The latter is an originally empirical relation describing the increase of the number of logic subpackages contained in the package. The rule was shown by Russo and co-workers [6], using partitioning experiments, to be a consequence of the structure of logic and the desire to optimize performance in the presence of limited package

connector counts. The net of these results is that wiring complexity increases significantly with logic complexity, at least up to that packaging level where distinct subsystem functions begin to be recognizable.

Implicit in Donath's model is the realization that it is critically important for the layout designer (and the wiring algorithm) to take account of wiring demand in a *global* sense, at the top of the logic package hierarchy. Both automatic placement and automatic wiring programs making direct use of this understanding were written by Donath (unpublished), by Khokhani and co-workers (placement [7]), and by Chen, Feuer, Nan, and co-workers (wiring [8]). While this was being done, a probabilistic model of logic wiring connections was worked out by Heller, Mikhail, and Donath [9]. This model used Donath's wire length estimate and made available quantitative early package design for proper wiring capacity. It makes possible wireability predictions, for example, in the experimentally optimal situation where the automatic programs can be used with minimum attention to electrical constraints, followed by manual, interactive editing. In the model, the assumption

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was made that so-called "programmable vias" were always available when needed on the packaging image when wires must pass from one package wiring plane to another.

One purpose of the present paper is to present some empirical evidence on the value of such programmable vias relative to the more traditional "fixed-via" pattern often chosen in packages higher than chip level. The main advantages of fixed vias come from lower manufacturing cost and greater simplicity, at the expense of giving less help to wiring programs. The present work reports experiments which compare the effectiveness of fixed *versus* programmable vias as seen by a wiring program which uses a global router followed by a line-packing routine and a final restricted maze-runner. The principal result of the experiments is that reduced overflow count, measuring wiring success, is displayed using programmable vias. The reduction can be as much as a factor of two where there are as many as six wiring tracks per pin channel. The improvement is less marked when there are fewer tracks per pin channel. An intermediate type of via (the "segmented" via), fixed in location but connecting only members of a plane wiring pair, is found to give results intermediate between fixed and programmable vias.

Another important aspect of the via dependence of logic package wiring, not specifically treated in the paper, is the relative importance of *overall* and *local* fixed-via supply. W. Vilkelis [10] has pointed out that with a fixed-via pattern, one needs a uniform distribution of via holes, between one and two per pin on average, for best wireability of the grid.

Another set of our experimental results deals with the wiring effects of changing the availability to pin connection under the subpackages of global "pass-through" wiring tracks. The wiring programs make considerably less effective use of tracks which "pass by" the subpackages, or of "jumper" tracks, which run from pin to pin. Overflow count is found to rise appreciably when the proportion of pass-by and jumper tracks to pass-through tracks is made to grow, with fixed total wiring capacity.

Finally, the paper makes a comparison of two different wiring program arrangements on one of the package images. The first uses a sequence of global routing and line-packing techniques, followed by use of a restricted maze runner. The second uses the restricted maze runner alone, but with successive passes increasing the freedom of access of the routine to vias and wiring space. The recent work of H. So and of E. Kuh and co-workers presents theoretical limits and algorithmic techniques for minimizing the via demand by use of ordering the routing in single-channel rows [11-13]. This work is related to the earlier algorithmic techniques of channel-packing, appropriate for situations where via

density is plentiful [14, 15]. Our experience, nevertheless, suggests that realistic consideration of dense two-dimensional global wiring demand will increase via usage very significantly over the minimum value achievable during routing of wires in a single channel.

2. The experimental framework

In the experiments reported here, some of the most basic trade-offs in wiring capacity are tested, using two types of wiring programs and several via types, as well as several different subpackage pin dispositions and a number of contrasting wiring arrangements.

• Method of placement

The placement of subpackages on the module has been done manually; the average length of the wires results from this placement and from the assignment of pins, which has been done randomly within each subpackage image. The tables of results presented later indicate that the average wire length exceeds, by a factor of 35-50%, the value one might obtain from the most effective available automatic placement and connector assignments [2-4, 7, 8]. In practice, it is hard to avoid this length penalty, or indeed, a significant amount of manual intervention in higher-level package placement and pin assignment. This comes from the frequent necessity for *a priori* "bottom-up" package pin assignment, the difficulties of wire "escape" on the package from underneath a pin-heavy subpackage image, and the paramount influence on wiring lengths of the electrical and timing constraints throughout the packaging hierarchy.

• Description of wiring program used

The general principle for wiring programs which gives the best routing results for the package images used here was originally developed for use in automatic wiring of chips [7, 8]. A global evaluation of wiring demand against wiring capacity is made by the initial pass of the algorithm, looking at the linear boundaries of a checkerboard pattern of squares on each plane pair. Then the connections of the nets (A net is a set of pins wired together to be electrically common. The term "connection" is reserved for a net segment connecting two pins.) are displaced in the *x* or *y* or the *z* direction (if more than one plane pair is available) to achieve a smooth distribution of wiring demand from square to square throughout the image.

It is customary to report wiring results in terms of the number and length of connections completed and number and minimum length of connections left unwired by the program. A complete global pass should also look at via usage in the *x-y* planes, and try to smooth it with a weight depending upon the cost in extra wiring length and demand. The necessity for the program to have such a global, via-smoothing capability is usually minimized by taking a suffi-

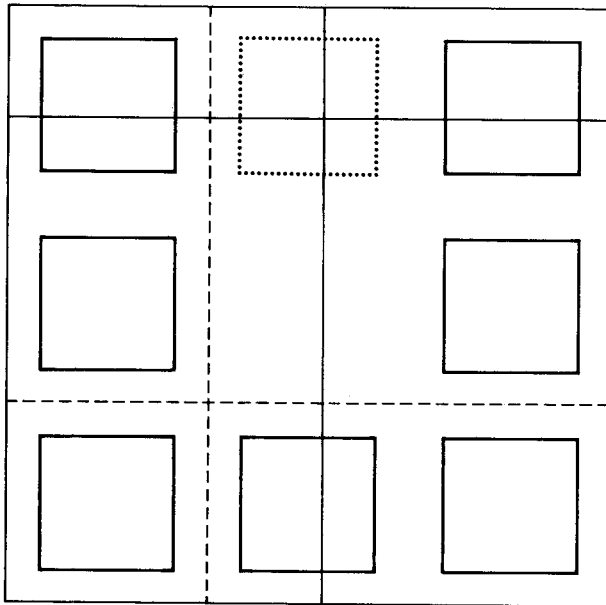


Figure 1 Arrangement of eight subpackages, with *edge* connectors (·) on the package to be wired. Solid line (—) denotes example of "pass-through" global track. Dashed line (---) denotes example of "pass-by" global track.

cient supply of vias throughout the image. In computer logic networks, the average number of pins per net varies from two to three. The average number of vias per used pin in a properly via-stocked pin matrix lies between 0.5 and 1.5, if the wiring capacity is chosen adequately large [9].

After the global pass or passes have been completed, a line-packing technique can be used effectively. With such techniques and a sorting procedure, one can remove cycles and other conflicts in track demand in one or a small adjacent group of channels on one wiring plane pair at a time [8, 14, 15].

Finally, one can invoke a maze-running procedure [1], with sequentially increasing permitted "windows" of operation in the x - y plane with controllable time of search and with controllable via usage per net. Overflows, *i.e.*, wires not embedded by the sequence of program routines, are listed and left for interactive manual embedding on the image, or relegated to the category of discrete wires to be completed *outside* the printed wiring levels. Because there are no electrical or performance constraints on wire ordering or length, the overflow count is chosen as a measure of wiring difficulty.

3. Description of the wiring images and experiments

In this section, we discuss various measures of the quality of the subpackage connector matrix and of the package wiring track- and via-matrices.

The most important single package variable determining wiring success is the wiring capacity. This is the total length of wire which could be fitted into the package if all tracks were completely used throughout their length. Earlier work by two of the present authors and Donath [9] showed that, when wiring demand (total wire length of projected "Manhattan" routes from used pin to used pin in all connections), the number of such connections per subpackage, and total subpackage count are known, a probabilistic model for wiring success can be used to make usefully accurate predictions.

Unfortunately, it is not always possible to put wiring tracks near enough to the subpackage pins to be successfully connected by wires. And the vias permitted in some packages may not be adequate in number, or located near enough to some of the wiring tracks where they are needed. The analytic work earlier referred to [9] was able to assume, as in the masterslice (gate array) chip there modeled, that pins per subpackage (there, a subpackage was a logic gate) were few in number and close to the wiring tracks. Vias were programmably located on the tracks where they were needed. Here, in contrast, we are investigating, on higher-level packages, a more complex situation. The subpackage pin count in our present experiments varies from forty-four (experiments A and B) to two hundred and fifty connectors in the most complex case (experiment D). With many connectors, their high concentration in a given area is important. In the experiments, two contrasting arrangements are studied: "edge" connectors at the periphery of the subpackages, and "area" connectors distributed over the entire region underneath the individual subpackages.

With each of these two connector arrangements, contrasting methods of providing wiring tracks must be studied. With one method, some wiring tracks pass globally from one side of the package to the other underneath the subpackages; global tracks also pass adjacent to these subpackages. With still another approach, some tracks stop at the periphery of the subpackages and resume on the other side. These latter tracks are referred to as "jumper" tracks. Whether one can simply add the capacities of each type of track in this case to obtain a meaningful "total" capacity is a question to be answered by experiment. In reporting results, we therefore separate the three types of track just referred to when giving capacity per subpackage.

Another subpackage parameter which requires study is the via type and distribution which we have already discussed.

We now describe the details of the series of experiments. In sets 3A and 3B, all vias used are programmable; the effects of subpackage pin location and track type are investi-

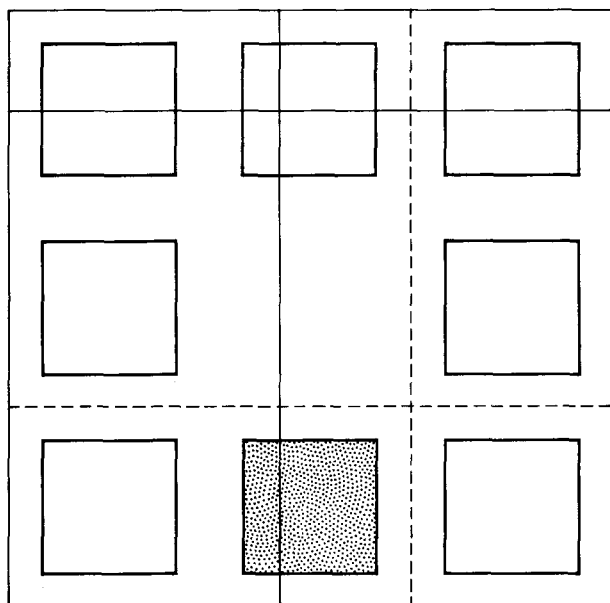


Figure 2 Arrangement of eight subpackages, with area connectors (•) on the package to be wired. Solid line (—) denotes example of "pass-through" global track. Dashed line (- -) denotes example of "pass-by" global track.

gated. In experiments 3C and 3D, the emphasis is on the relative effectiveness of fixed and programmable vias. In addition, different types of global tracks are also examined. We report the results of wiring program experiments on the images described here in a separate section. In all the experiments, wires going to package (as opposed to subpackage) connectors were eliminated. Wires to terminator resistors were also ignored. An increase of the overall average length of wires is the penalty in practical wiring situations for reducing the length of a minority of certain critical nets interconnecting subpackages which must be placed in specified relative locations to satisfy electrical or timing constraints on those critical nets.

• The 3A series of experiments

Eight subpackages were arranged symmetrically on a square planar wiring package with one horizontal and one vertical wiring plane. (The center position was open.) Each subpackage had 44 signal connectors for input and output signals. Programmable vias were used, and there was one "plane pair" for wiring: one plane for horizontal wiring, one plane for vertical.

Experiment 3A-1 In this arrangement (see Fig. 1), the input/output connectors of each subpackage were disposed around the edges of the subpackages. Each subpackage position had 16 vertical channels (one track per channel) running under the subpackage and ten vertical channels (one track per channel) on each side of each subpackage. A similar statement holds for the horizontal wiring plane.

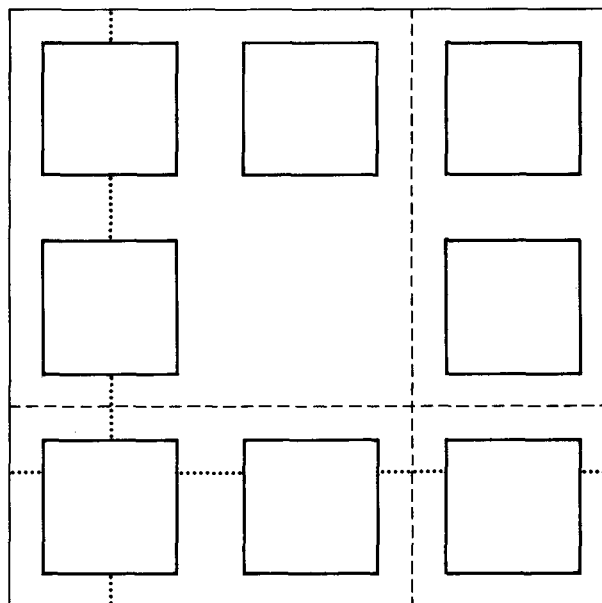


Figure 3 Arrangement of eight subpackages, with edge connectors (•) on the package to be wired. Dotted line (· · ·) represents "jumper" tracks, which do not pass under the subpackages. Dashed line (- -) represents "pass-by" global tracks.

Experiment 3A-2 In this arrangement (see Fig. 2), the input/output connectors were disposed randomly in 44 locations on a 17 by 17-position grid interpenetrated by the sixteen wiring channels (one track per channel). Again, there were ten wiring channels (one track per channel) at each side of each chip.

Experiment 3A-3 In this arrangement (see Fig. 1), the input/output connectors were disposed as in experiment 3A-1 at the edges of the subpackages. Here, however, 32 wiring tracks were arranged to pass under the subpackages at two tracks per channel. In addition, there were two extra tracks (see the extra channel at each side of each subpackage). Thus, the total wiring capacity (measured in tracks) per subpackage was the same as in experiment 3A-1, but the tracks were heavily concentrated under the subpackage.

Experiment 3A-4 In this arrangement (see Fig. 2), the input/output connectors were disposed as in experiment 3A-2 throughout the area under the subpackage. Here, however, 32 wiring tracks were arranged to pass under the subpackages, at two tracks per channel. In addition, there were two extra tracks per channel (one extra channel) at each side of each subpackage.

Experiments 3A-5, 3A-6, 3A-7, 3A-8, 3A-9, 3A-10 Here (Fig. 3), the input/output connectors were arranged as in Fig. 1, at the subpackage edges. In contrast with the earlier arrangements, there are global "pass-by" tracks and tracks which begin or end at the edges of the subpackage, "jumper"

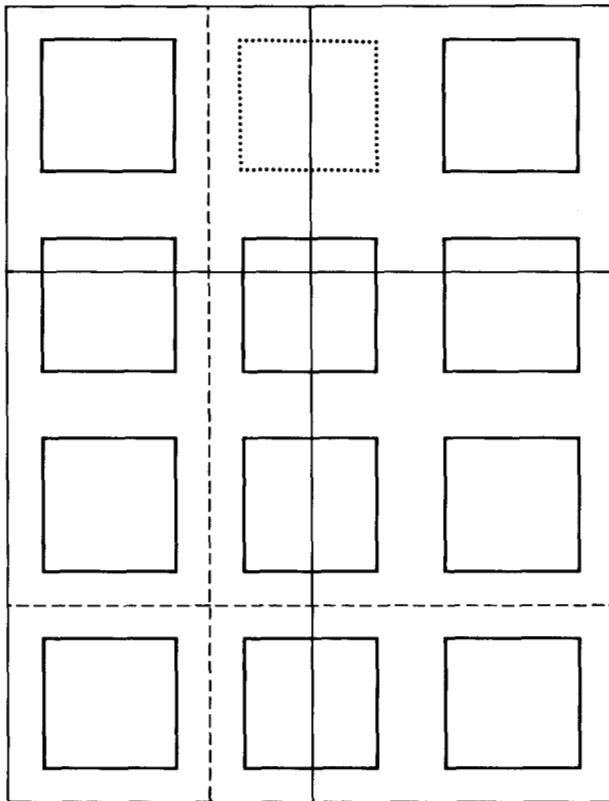


Figure 4 Arrangement of twelve subpackages, with *edge* connectors (·) on the package to be wired. Solid line (—) denotes example of "pass-through" global tracks. Dashed line (---) denotes example of "pass-by" global tracks.

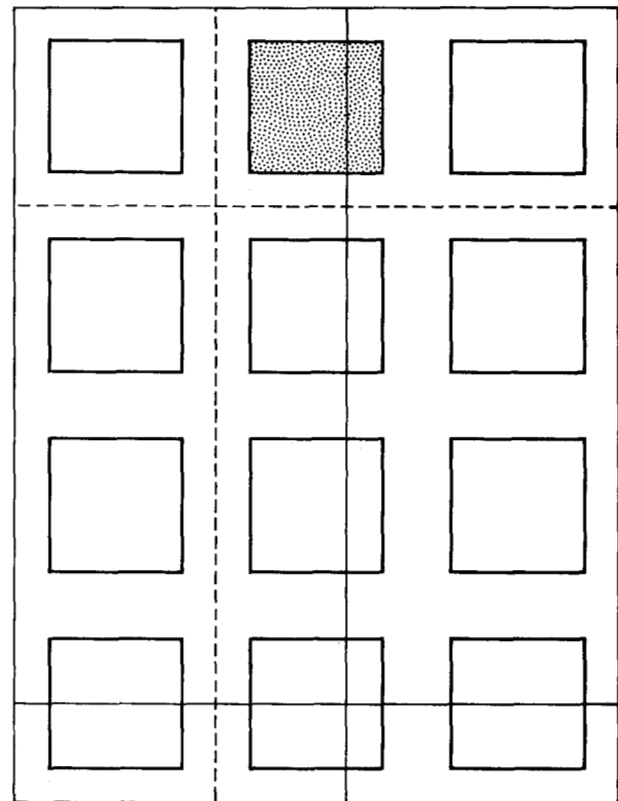


Figure 5 Arrangement of twelve subpackages, with *area* connectors (·) on the package to be wired. Solid line (—) denotes example of "pass-through" global tracks. Dashed line (---) denotes example of "pass-by" global track.

tracks. The numbers of global and jumper tracks were systematically varied. A series of six experiments was run starting with the largest numbers of both global and jumper tracks. Then either or both global and jumper track counts were decreased in step in successive experiments. In the first two of these experiments, there were 32 free vertical horizontal global tracks per subpackage, 16 to its right and 16 to its left. But the relative concentration of jumper tracks is varied by using two tracks per channel in the first experiment (3A-5), while one track per channel is used in experiment 3A-6. In each of experiments 3A-7, 3A-8, and 3A-9, there are 24 vertical (horizontal) global tracks per subpackage, 12 to the left and 12 to the right of each. The capacity of jumper tracks is computed from the number of tracks equivalent in length to global tracks. Thus, for example, in experiment 3A-6, there are actually 16 jumper tracks per subpackage, but the total length of the jumper tracks is shorter because they do not pass under the subpackages.

The relative concentrations of jumper tracks are again varied in these three experiments. In 3A-7, 3A-8, and 3A-9, there are one track per channel, two tracks per channel, and

three tracks per channel, respectively. In all these experiments, the number of channels measuring the width of the subpackage is unchanged. Finally, in experiment 3A-10, there are 18 vertical (horizontal) global tracks per subpackage, nine on each side. Again, jumper concentration is increased by using five tracks per channel in the regions abutting the subpackage.

• The 3B series of experiments

The 3B series of experiments is essentially similar to the 3A series, except that here 12 subpackages are arranged in a three by four matrix on a package larger than that for 3A, but still with one wiring plane pair and programmable vias. Figures 4, 5, and 6 show the arrangements corresponding in the 3B series to Figs. 1, 2, and 3 in the 3A series.

• The 3C series of experiments

In this series of experiments, the subject studied was the effect of disposition of fixed vias running through the package.

Experiment 3C-1 The subpackages were disposed on a six-by-six square array, each subpackage having 96 signal

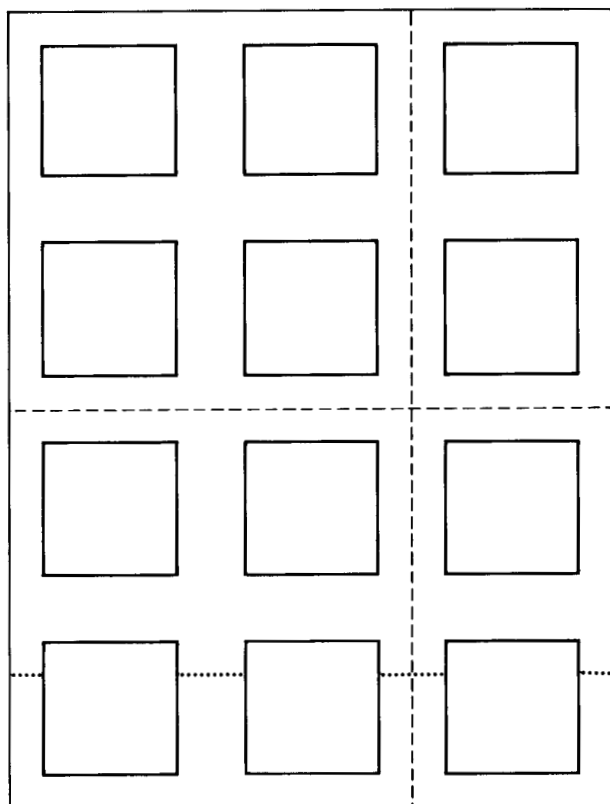


Figure 6 Arrangement of twelve subpackages with edge connectors, as in Fig. 4, on the package to be wired. Dotted line (· · ·) denotes "jumper" track, which does not pass under the subpackages. Dashed line (- -) denotes example of "pass-by" global tracks.

connectors distributed on a 17 by 17 array of fixed vias. There was one wiring track per channel and a total of six signal wire plane pairs (Fig. 7).

Experiment 3C-2 The same experiment was run as in 3C-1, except that the via locations were reduced in number (Fig. 8), so that running diagonally, one third of the via positions were reserved for power and ground, one third for signals, and one third for fixed vias. One wiring track per channel was used. The program worked with only one plane pair at a time, and roughly equal numbers of connections were allocated to each plane pair.

Experiment 3C-3 Here the same arrangement was used as in 3C-2, except that seven plane pairs were allotted instead of six for wiring.

• The 3D series of experiments

In this set of experiments, a larger image than that in 3C was studied, but here the comparison is between the use of programmable vias and the use of fixed vias in the package image. A five-by-five rectangular matrix of subpackage locations was created on a planar package. On these loca-

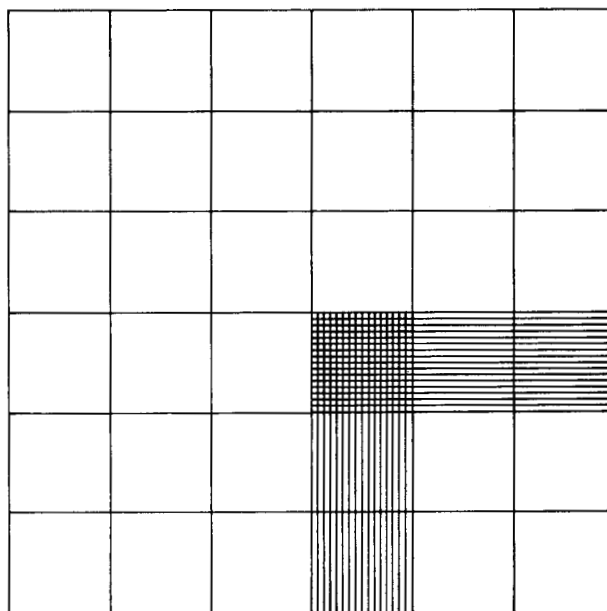


Figure 7 Arrangement of thirty-six subpackages with area connections arising from a 17×17 -pin matrix of which 96 signal pins are used and are available via positions redistributed from overlying planes to the uniform pin-channel matrix shown. Sixteen global channels pass under each subpackage location in each horizontal and vertical wiring plane.

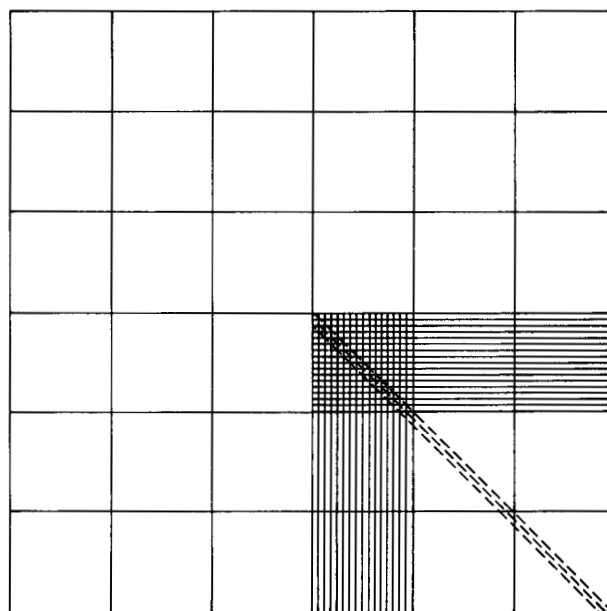


Figure 8 Arrangement of thirty-six subpackages as in Fig. 7. Here the uniform pin matrix has been subdivided along diagonal lines which repeat in a sequence of three types: (a) signal pins, (b) signal vias, (c) power pins. Again, 96 signal pins from each 17×17 -subpackage group are used.

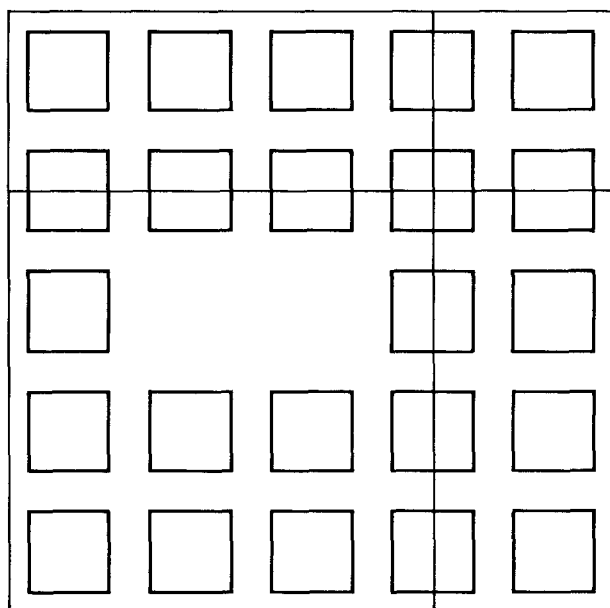


Figure 9 Arrangement of 23 subpackages on a 5×5 matrix, with a 41×41 -channel matrix under each subpackage, with one channel per subpackage on each side of each subpackage. The number of tracks per channel is varied in experiments.

tions, 23 subpackages were disposed, each with an average of 250 used input/output connectors. The latter were defined as a randomly chosen subset of a 42 by 42-pin submatrix lying adjacent to a 41 by 41-channel matrix (see Fig. 9). In the first three experiments of this section, a rectangular matrix of pins and channels was used, and programmable vias were defined as the program required them on the wiring tracks.

In the last four experiments of this section, diagonal rows of pins were interspersed with rows of power and signal vias and fixed via locations (except as noted below). Thus the image under the subpackage in the last four experiments was essentially similar to that in Fig. 8. In arrangement of the subpackages, on the other hand, the same array was used as in the first three experiments of this section. Programmable or fixed vias were used, as noted in discussions of the individual experiments.

Experiment 3D-1 Three plane pairs of wiring were provided with three tracks per channel, a 41 by 41-channel matrix and three additional tracks (one extra channel) between subpackages. Programmable vias were used.

Experiment 3D-2 The same set-up was used as in case 3D-1, except that there were two plane wiring pairs with four lines per channel, and four extra tracks (one extra channel) between subpackages. Programmable vias were used.

Experiment 3D-3 The same channel matrix was used as in case 3D-1 underneath the subpackages, with three plane wiring pairs, two lines per channel, and programmable vias. In this case, however, there were 115 tracks between each pair of subpackages on each of the vertical wiring planes and 90 tracks between each subpackage pair on horizontal wiring planes. Programmable vias were used.

Experiment 3D-4 The image of the package under the subpackage is similar to that in Fig. 8. The diagonal fixed-via grid was used and no programmable vias were employed. Eight plane wiring pairs were used with one track per channel, and one channel (track) was taken between subpackages.

Experiment 3D-5 The same image was used as in experiment 3D-4, but nine plane pairs were used instead of eight.

Experiment 3D-6 In this experiment the same subpackage and package images were used as in 3D-4 and 3D-5, but no use was made of the fixed vias on the diagonal via/pin grid. Instead, programmable vias on the tracks themselves were used as needed by the program. Eight plane wiring pairs were used.

Experiment 3D-7 The same experiment was performed as in 3D-6, except that nine plane wiring pairs were employed.

4. Description of experiments demonstrating program effectiveness in various track and via configurations

The image and experiments described for the 3C series served as the basis for a deeper investigation of the effects of track density and via type in their interaction with the overall tactics one can use with the wiring program. Five different sets of experiments were run. On the fixed through-via grid the wiring program was first directed to use global wiring followed by line packing (as discussed in Section 2) and thereafter to use the line-probe maze runner in several successive passes with increasing via count and window made available. With this same sequence of wiring instructions, the program was then directed to run on a two-plane-pair wiring matrix, with three tracks per channel, and finally, on the same matrix with one plane pair and six tracks per channel. This is experiment 4A.

Next, instead of using an image with fixed through vias, the vias were *segmented* on fixed locations to individual plane pairs. This is experiment 4B.

To test the effectiveness of the maze runner alone, a third set of runs was carried out, on all three track-plane-pair arrangements with segmented vias. This is experiment 4C.

Next, the fixed-via grid was ignored and the programmable vias in the wiring track themselves were used. The

same comparisons of wiring program sequence were carried out on all three wiring images. These are experiments 4D and 4E.

In actuality, there were several parameters internal to the wiring program chosen for the use of the global and line-pack algorithms; these differed to suit the fixed-via and the programmable-via situations.

For package images with fixed vias, the global and line pack program was limited to paths with less than three vias: Each channel (*i.e.*, including the tracks between adjacent rows of pins) was rerouted each time it was desired to route a new wire through the channel. In this experiment, the vias were assumed to interconnect only one plane pair. The line probe maze runner was used to try to route overflows after the line-pack algorithm had completed its attempt.

When the statistics refer to runs with "non-line packing," only the line probe maze runner was used. In all maze runner passes, the connections were sorted short to long and were tried in that order. Also, connections were not retried once made.

Before wiring runs were made, controls over the maze runner were set as parameters to be automatically used by the program. There were several major and several minor controls: One major control selected a particular plane pair or an order for all plane pairs in succession; another chose a fixed frame or window on both planes within which the maze runner was restricted for each connection. Minor controls included specifying the maximum number of vias to be used in a connection, and the "swath" of channel length for the minimum starting length of a connection, together with a chosen width. A final parameter chose a maximum value for the CPU time the maze runner was permitted for each connection.

For packages with programmable vias, a different global and line-pack algorithm was used. This algorithm assigned each connection to a plane pair, and the global and line-pack algorithms were run on a plane pair at a time. Each plane pair is divided into rectangles. The global algorithm indicated the rectangles each connection should pass through, not limiting the number of vias to be used. One row or column of rectangles was packed at a time. Then the line probe maze runner was used to try to route overflows. Fixed parameters were used in each series of experiments.

5. Presentation and discussion of results

The results of the sets of experiments are presented in the tables to follow. For convenience, we first discuss sets 3A and 3B as a group; then we summarize general conclusions after discussing sets 3C and 3D. Finally, we present results

from the experiments in Section 4 dealing primarily with the interplay of wiring programs, via usage, and wiring track density.

In the tables, the average lengths of connections $\bar{R}$ are presented in terms of subpackage "pitches"; one pitch equals the center-to-center distance of two adjacent subpackages. Lengths are expressed in track count along a line running perpendicular to the track direction. The prefix "Manhattan" refers to the distance computed as rectangular minimum distance from pin to pin of each connection. The "actual" average length is that computed from the result of the wiring program's actions, again in rectangular segments.

Wiring capacity (last row in the tables) is expressed in terms of the spacing from subpackage center to subpackage center as measured in track count along a line running perpendicular to the tracks. The three components that comprise the wiring capacity are

1. Wiring capacity of global tracks passing underneath the subpackage ("pass-through" or PT tracks);
2. Wiring capacity of global tracks *not* passing underneath the subpackage ("pass-by" or PB tracks); and
3. Wiring capacity of non-global tracks ("jumper" or J tracks).

Tables 1 and 2 summarize the results of wiring runs using the global, line-packing, and maze-running routines on the 8- and 12-subpackage boards.

• Results of the 3A and 3B experiment series

The results for the 3A and 3B experiments are described together, since they represent similar wiring problems except for total subpackage and net count. A very striking result is seen by comparing experiments 3A-1 and 3A-3, for example, with experiment 3A-8. The same contrast is seen between 3B-1 and 3B-3 in comparison with 3B-8. The increase in overflow count for 3A-8 and 3B-8 in contrast with their pairs of partners can be ascribed to the reduced efficiency of wiring tracks which do not run all the way across the planar supporting package, underneath the subpackages. Even though the total wiring track capacity per chip changes very little (32 *versus* 33.5), the number of global tracks running underneath the subpackages has been decreased in 3A-8 and 3B-8 by 25% (32 to 24). The deleterious result is twofold: First, the overflow count goes from zero or one to 18 (3A-8) and 33 (3B-8). Second, the failed connections have almost 75% greater average length, which implies that manual embedding techniques would have much greater difficulty (they would use much more design time).

The point discussed above is emphasized by noting experiments 3A-7 (3B-7), 3A-9 (3B-9), and 3A-10 (3B-10). In

Table 1 Wiring results on 8-subpackage board.

Experiment no.	3A-1			3A-2			3A-3			3A-4			3A-5			3A-6			3A-7			3A-8			3A-9			3A-10																																																			
No. nets	←—————99————→																																																																														
No. connections	←—————185————→																																																																														
Manhattan $\bar{R}$ (total)	1.62			1.57			1.66			1.61			1.61			1.61			1.62			1.61			1.63			1.65																																																			
Manhattan $\bar{R}$ (compl.)	1.61			1.43			1.66			1.61			1.61			1.6			1.43			1.47			1.45			1.34																																																			
Manhattan $\bar{R}$ (fail.)	2.9			2.38			—			—			—			1.0			3.52			2.89			3.45			2.84																																																			
Actual $\bar{R}$ (compl.)	1.88			1.74			1.77			1.74			2.0			2			1.87			1.97			1.82			1.63																																																			
No. overflows	1			28			0			0			0			1			17			18			17			38																																																			
	PT	PB	J	PT	PB	J	PT	PB	J	PT	PB	J	PT	PB	J	PT	PB	J	PT	PB	J	PT	PB	J	PT	PB	J	PT	PB	J																																																	
Wiring capacity per subpackage location per plane	16			20			16			20			32			4			0			32			4			0			32			16			0			32			10.67			0			24			9.6			0			24			13.7			0			24			16			0			18			14.7

Table 2 Wiring results on 12-subpackage board.

Experiment no.	3B-1			3B-2			3B-3			3B-4			3B-5			3B-6			3B-7			3B-8			3B-9			3B-10		
No. nets	←—————101————→																													
No. connections	←—————234————→																													
Manhattan $\bar{R}$ (total)	1.76		1.7		1.78		1.76		1.76		1.75		1.76		1.75		1.77		1.78											
Manhattan $\bar{R}$ (compl.)	1.75		1.57		1.78		1.76		1.70		1.74		1.52		1.48		1.53		1.36											
Manhattan $\bar{R}$ (fail.)	2.9		2.5		3.7		—		3.97		1.94		3.56		3.43		3.6		3.1											
Actual $\bar{R}$ (compl.)	1.94		1.9		1.95		1.95		2.09		2.18		1.90		1.94		1.84		1.6											
No. overflows	1		32		1		0		3		9		28		33		27		56											
	PT	PB	J	PT	PB	J	PT	PB	J	PT	PB	J	PT	PB	J	PT	PB	J	PT	PB	J	PT	PB	J	PT	PB	J	PT	PB	J
Wiring capacity per subpackage location per plane	16	20	0	16	24	0	32	4	0	32	4	0	0	32	16	0	32	10.67	0	24	9.6	0	24	13.7	0	24	16	0	18	14.7

Table 3 Wiring results from a six-by-six-subpackage array on a board.

Experiment no.	3C-1	3C-2	3C-3
No. nets	←—————1123————→		
No. connections	←—————2313————→		
Manhattan $\bar{R}$ (total)	1.96	1.96	1.97
Manhattan $\bar{R}$ (compl.)	1.74	1.69	1.83
Manhattan $\bar{R}$ (fail.)	4.44	4.31	4.67
Actual $\bar{R}$ (compl.)	2.17	1.91	2.06
No. overflows	189	244	113
Wiring capacity per subpackage for all planes	204	204	238

3A-7 (3B-7) and 3A-9 (3B-9), neither reducing nor adding jumper tracks to the 24 global tracks has appreciable effect on overflow count. Decreasing the global underpass tracks to 18, on the other hand, in experiment 3A-10 (3B-10) roughly doubles the overflow count. Finally, experiments 3A-5 (3B-5) and 3A-6 (3B-6) show that when one increases the global underpass tracks to the same value as in 3A-3 (3B-3), the

overflow count is restored to a small or a negligible value, one very weakly dependent on the number of jumper tracks when those vary from 10.67 to 16.

A separate insight from those just discussed is gained by comparing the results of experiment 3A-1 to that of 3A-2 (or of 3B-1 to 3B-2). Here we can see the influence of the difficulty of wires in "escaping" from an area of high-level concentration. The overflow count is higher in 3A-2 than 3A-1 and likewise much higher in 3B-2 than in 3B-1. The escape is more difficult when the nets originate throughout the area of a subpackage than when they emerge from the edges of the subpackage. A compensating effect can be seen in comparing 3A-2 and 3A-4 (or 3B-2 against 3B-4). Here the escape problem is eased by concentrating a sufficient number of global tracks underneath the subpackages (in 3A-2 and 3B-2). Thus we have shown that the escape problem is basically a localized phenomenon associated with the balance of local wiring demand and capacity near the pins of the subpackages.

Table 4 Wiring results for 23 subpackages on a five-by-five-subpackage array on a board.

Experiment no.	3D-1	3D-2	3D-3	3D-4	3D-5	3D-6	3D-7
No. nets	1709						
No. connections	4053						
Manhattan $\bar{R}$ (total)	2	2	2	2	2	2	2
Manhattan $\bar{R}$ (compl.)	2	1.96	1.95	1.95	2.0	1.9	1.96
Manhattan $\bar{R}$ (fail.)	5.7	4.12	2.88	4.28	—	4.30	4.62
Actual $\bar{R}$ (compl.)	2.05	2.02	2.03	2.09		2.0	1.97
No. overflows	1	50	53	85	0	180	65
Wiring capacity per subpackage location for all planes	756	672	1104*	672	756	672	756

*The number for the wiring capacity for case 3D-3 is made up of two: the first (492) gives the number of global (pass-through) tracks under each subpackage; the second (612) gives the number of global (pass-by) tracks per subpackage lying between adjacent subpackages.

• Results of experiments 3C

The results of the experiments 3C-1, 3C-2, and 3C-3 are tabulated in Table 3. Comparing 3C-1 and 3C-2, we see the effects of sharply reducing the count of fixed vias, the only type made available. The overflow count is seen to rise sharply by about 30%. One can cure the problem by going to another plane pair. As we see from 3C-3, this reduces the overflow count by more than a factor of two. The cost of the extra plane pair must be balanced against a possible improvement in via capability.

• Results of the 3D experiment series

The 3D experiment series forms a more complex set than the 3C series and demonstrates the effects of programmable vias. The results are listed in Table 4. In experiments 3D-1 and 3D-2, we deal with a set of package wiring images in which we study the effects of using alternative wiring track configurations for the wiring problem. In effect, plane pairs are exchanged for tracks.

The reduced capacity in 3D-2 compared to 3D-1 increases the overflow count. In Section 4, further data on this problem are presented together with discussion of the results of using alternative wiring program tactics. Experiment 3D-3 shows what happens when the image of case 3D-1 is changed by removing one track per channel from each channel and putting large numbers of extra tracks between the subpackages. One notices that, even though track capacity per subpackage has been greatly increased, the overflow count has gone up. *This is due to the fact that the extra tracks are not where they are needed.* Note also that the actual length of the wires has gone way up, even though the length measured in pitches has remained the same. This experiment shows how to waste wiring space.

Experiments 3D-4 through 3D-7 display another type of problem. Here we are looking at an image like that in Fig. 7 or Fig. 8. Experiments 3D-4 and 3D-5 show the effect of

programmable vias on making the image wireable, as well as the benefit of an extra plane pair in 3D-5. In 3D-6 and 3D-7, on the other hand, there are fixed vias on one of every three diagonal lines, as shown in Fig. 8. We see a very noticeable degradation in wiring completion; even the extra plane pair in 3D-7 does not make up for fixed via scarcity and inaccessibility, as compared to programmable vias. Only one of every three grid points for pins or vias is a permitted via position.

One question concerning wiring capacity remains. It might appear that increasing global wiring capacity by increasing the number of plane pairs is equivalent to adding more tracks per channel with fewer plane pairs. It is easy to see that this could, at best, only be true if programmable vias could be used, since wiring in more than two tracks per channel would lead to difficulty of access to the central wires. The results of the experiments 3D-4, 3D-1, and 3D-2 show a possible trend toward favoring the "multi-track, few-plane-pair" wiring image over the "few-track, multi-plane-pair" alternative. The apparent discrepancy between 3D-2 and 3D-1 results from the extra capacity per subpackage in 3D-1. We offer an explanation for then taking the trend as slightly favoring the "multi-track, few-plane-pair" image. If, for example, segments of a path have to be wired on the same plane pair, this can cause a conflict between segments of different connections in the one-track-per-channel, two-plane-pair situation. Such a conflict need not arise when two tracks per channel are available in a single plane pair. Of course this argument would not apply if the program could look at all available planes of a multi-plane-pair package before assigning segments to a particular plane. The next section contains more data on the plane-pair versus tracks-per-channel question.

• Results of experiments on wiring program effectiveness in various track and via configurations

The five sets of experiments in Section 4 were done in a wiring image similar to that used in the 3C series of

Table 5 Wiring results for a six-by-six-subpackage set, each on a 17×17 -channel matrix, with fixed vias passing through all planes. Use of global wiring, followed by line packing and a maze runner (experiment 4A).

Experiment no.	4A-1	4A-2	4A-3
No. nets	1123		
No. connections	2313		
No. tracks/channel	1	3	6
No. signal plane pairs	6	2	1
No. vias available	5236		
Manhattan $\bar{R}$ (total)	1.96		
in subpackage pitches			
Manhattan $\bar{R}$ (compl.)	1.69	1.67	1.66
in subpackage pitches			
Manhattan $\bar{R}$ (fail.)	4.86	4.24	3.75
in subpackage pitches			
Actual $\bar{R}$ (compl.)	1.98	1.89	1.85
No. vias used	2974	2720	2606
No. overflows	193	253	328
Wiring capacity per subpackage for all planes (in tracks)	204		

Table 6 Wiring results for a six-by-six-subpackage set, each on a 17×17 -channel matrix, with fixed segmented vias (connecting two planes only). Use of global wiring, followed by line packing and a maze runner (experiment 4B).

Experiment no.	4B-1	4B-2	4B-3
No. nets	1123		
No. connections	2313		
No. tracks/channel	1	3	6
No. signal plane pairs	6	2	1
No. via locations available	5236×6	5236×2	5236×1
Manhattan $\bar{R}$ (total)	1.96		
in subpackage pitches			
Manhattan $\bar{R}$ (compl.)	1.71	1.69	1.66
in subpackage pitches			
Manhattan $\bar{R}$ (fail.)	5.1	4.33	3.75
in subpackage pitches			
Actual $\bar{R}$ (compl.)	2.0	1.91	1.85
in subpackage pitches			
No. vias used	3139	2840	2606
No. overflows	172	230	328
Wiring capacity per subpackage for all planes (in tracks)	204		

experiments. Each subpackage has allotted to it a 17×17 -channel array, and there is a 6×6 -subpackage matrix on the planar package in question. There are 1123 nets and 2313 connections. The tables corresponding to Section 4, labeled 5 through 9, deal with the various cases studied.

One conclusion from these experiments is that the trend in overflow count is *upward*, from the six-plane-pair arrangement with one track per channel to the single-plane-pair set-up with six tracks per channel, in experiments 4A, 4B,

Table 7 Wiring results for a six-by-six-subpackage set, each on a 17×17 -channel matrix, with fixed segmented vias (connecting two planes only). Use of maze-runner program only (no global wiring or line-pack routines) (experiment 4C).

Experiment no.	4C-1	4C-2	4C-3
No. nets	1123		
No. connections	2313		
No. tracks/channel	1	3	6
No. signal plane pairs	6	2	1
No. via locations available	5236×6	5236×2	5236×1
Manhattan $\bar{R}$ (total)	1.96		
in subpackage pitches			
Manhattan $\bar{R}$ (compl.)	1.70	1.72	1.67
in subpackage pitches			
Manhattan $\bar{R}$ (fail.)	5.28	4.01	3.5
in subpackage pitches			
Actual $\bar{R}$ (compl.)	1.94	1.87	1.8
in subpackage pitches			
No. vias used	2415	2185	2005
(estimated)	(estimated)	(estimated)	(estimated)
No. overflows	169	239	368
Wiring capacity per subpackage for all planes (in tracks)	204		

4C, and 4D tabulated in Tables 5-8. In contrast, the opposite trend is seen in the overflow result in experiments 4E, tabulated in Table 9. (Even within Table 9, however, the average length of the overflows goes down as fewer plane pairs are used, in agreement with results in the other tables.) The most significant reason for the partially contrary trend of overflow count in Table 9 is that the line-pack algorithm, as written, does not work effectively when there are only a small number of lines per channel. For cycles and other conflicts to be resolved (see the discussion in Section 2), a larger number of parallel tracks must be simultaneously available to the line-pack program. Possibly the use of a multi-channel line-pack window would give improved results when there are only a small number of tracks per channel.

In order to show further the contrast in the working of the wiring programs with and without global routing and line packing, Tables 10 and 11 are shown. The comparison is strongly influenced by the policy of sorting from short to long connections while operating the maze runner, together with the policy of completing all wires possible on the first plane pair, then passing to the next, and so on. With the global routing, a "pre-global" partitioning of wires to planes is also used to avoid cycles. This gives a more even distribution of wires over the planes in experiments 4D1 and 4D2, as compared to 4E1 and 4E2.

Overall, one can see that the combination of program-mable vias with global routing and line packing before maze

Table 8 Wiring results for a six-by-six-subpackage set, each on a 17×17 -channel matrix, with programmable vias (connecting two planes only, on wiring tracks). Use of global wiring, followed by line packing and maze-running routines (experiment 4D).

Experiment no.	4D-1	4D-2	4D-3
No. nets	← 1123 →		
No. connections	← 2313 →		
No. tracks/channel	1	3	6
No. signal plane pairs	6	2	1
No. via locations available	← very large →		
Manhattan $\bar{R}$ (total) in subpackage pitches	← 1.96 →		
Manhattan $\bar{R}$ (compl.) in subpackage pitches	1.74	1.83	1.87
Manhattan $\bar{R}$ (fail.) in subpackage pitches	4.44	3.56	3.21
Actual $\bar{R}$ (compl.) in subpackage pitches	2.17	2.09	2.05
No. overflows	189	168	159
Wiring capacity per subpackage for all planes (in tracks)	← 204 →		

Table 9 Wiring results for a six-by-six-subpackage set, each on a 17×17 -channel matrix, with programmable vias (connecting two planes only, on wiring tracks). Use of maze-runner program only (experiment 4E).

Experiment no.	4E-1	4E-2	4E-3
No. nets	← 1123 →		
No. connections	← 2313 →		
No. tracks/channel	1	3	6
No. signal plane pairs	6	2	1
No. via locations available	← very large →		
Manhattan $\bar{R}$ (total) in subpackage pitches	← 1.96 →		
Manhattan $\bar{R}$ (compl.) in subpackage pitches	1.70	1.68	1.64
Manhattan $\bar{R}$ (fail.) in subpackage pitches	5.28	5.21	4.74
Actual $\bar{R}$ (compl.) in subpackage pitches	1.94	1.84	1.71
No. overflows	169	185	239
Wiring capacity per subpackage for all planes (in tracks)	← 204 →		

Table 10 Distribution of actual (routed) connection length $\bar{R}$, measured in subpackage pitches, over the plane pairs available, as created by the two types of wiring program sequence, using programmable vias (taken from experiments 4D, E).

Package description	Experiments 4D-1, 4D-2: Global wiring, line packing, maze runner using programmable vias			Experiments 4E-1, 4E-2: Maze runner only using programmable vias		
	Plane-pair number (increasing away from sub-packages)	Number of connections on that plane pair	Average actual (routed) connection length ($\bar{R}$) meas. in subpkg-subpkg pitches	Plane-pair number (increasing away from sub-packages)	Number of connections on that plane pair	Average actual (routed) connection length ($\bar{R}$) meas. in subpkg-subpkg pitches
Six plane pairs, one track per channel	1	502	1.43	1	915	0.69
	2	348	2.12	2	406	1.49
	3	302	2.41	3	287	1.99
	4	279	2.61	4	198	3.58
	5	304	2.45	5	179	4.3
	6	389	2.08	6	159	5.07
Two plane pairs, three tracks per channel	1	1148	1.87	1	1565	1.15
	2	997	2.25	2	563	3.67

running results in the best (lowest) overflow counts. And it is probable that the higher the number of plane pairs (*i.e.*, the smaller the number of tracks in a channel), for fixed total capacity, the more iterations are required. Possibly a different grouping of channels should also be considered as suggested earlier, during each line-packing iteration of the global and line-pack programs.

Wherever the maze-runner completion rate becomes a dominant influence, we can expect an increase in plane pairs to be more beneficial than an increase in the number of tracks per channel, for equal wiring capacity added, with use of programmable vias. The contrary will be true for situations where global routing and line packing dominate the routing.

Table 11 Distribution of actual (rounded) connection length $\bar{R}$, measured in subpackage pitches, over various length ranges, as created by the two types of wiring, using programmable vias (taken from experiments 4D, E).

Connection length in subpkg-subpkg pitches	Six plane pairs, one track per channel				Two plane pairs, three tracks per channel			
	Maze runner only		Global wiring line placing, maze running		Maze runner only		Global wiring line packing, maze running	
	Number of connections	Percent of total	Number of connections	Percent of total	Number of connections	Percent of total	Number of connections	Percent of total
≤ 1 pitch between	562	26	538	25	693	33	549	25
(1-2)	593	28	557	26	517	24	640	30
(2-3)	482	22	67	22	502	24	471	22
(3-4)	356	17	300	14	298	14	259	12
(4-5)	114	5	140	7	86	4	109	5
(5-6)	33	2	74	4	30	1	57	3
(6-7)	3		31	2	2		33	2
(7-8)			17				16	1
(8-10)							11	

With fixed vias, the benefits of global wiring and line packing are less substantial or actually negative, in the images studied, if we look only at overflow count. But a secondary benefit is still found, if we look at the *average length $\bar{R}$* of the overflows to be embedded. This length is substantially smaller when global routing and line packing are used prior to use of the maze runner. Embedding of overflows is then substantially easier. Overall, the ratio of overflow wire length to average wire length varies between two and three. It usually lies on the lower side of the range when line packing is used. The average predicted Manhattan length of completed wires is larger when global wiring and line packing are used because more long wires were completed by the program.

The actual value of the ratio of average wire length to predicted average wire length varies from 1.05 to 1.25. The high side of this range is usually associated with the use of global routing and line packing. This is closely connected with the ability of the global router to trade off increased wire length for reduction of wiring congestion, as already seen by comparison of the actual average length of completed connections to their predicted average based upon rectangular segments (Manhattan length).

The fixed-via arrangement leads to a lower value of average wire length than the programmed-via arrangement in the same plane-pair and track-per-channel arrangement, essentially because fewer of the long wires are completed.

6. Conclusions

In this study of a range of package wiring images, the results of using two types of wiring programs were investigated. Among the package variables studied were the number and type of vias (fixed and programmable) and the number of wiring planes *versus* the number of wiring tracks per channel. A compromise had to be struck between the number of experiments done and the variation of the relevant parameters.

It was found that the use of global routing, followed by line packing and then restricted maze running, provided fewest overflows (the most direct measure of wiring success) and a tendency to *shorten* overflows. Programmable vias (as against fixed vias) made possible best use of many tracks per channel as against many wiring plane pairs. Use of programmable vias was roughly equivalent, in some cases, to as much as one plane pair as shown by the comparison of experiments 3D-4 and 3D-8 or of 3D-6 and 3D-7. Whatever the via type used, more than one available via per used pin ought to be present. Also noted were the effects of the different via configurations and the alternative programs on the average length of completed connections as well as overflow connections.

The effect of wiring track accessibility to subpackage pins was also studied. The optimum arrangement spread these pins widely (whether over an area or a periphery) and required global tracks passing under the subpackage image

and extending continuously from one side of the package to the other. A 50% increase in the number of global tracks outside the subpackage images still did not give as good wireability as having all global tracks underneath that image. So-called "jumper" or short pin-to-pin tracks were of limited value in relation to their length, as compared to global tracks. It is probably true that still further improvement of the wiring program would entail a more flexible balance between wire length and wire congestion, perhaps indicated by a parameter or parameters relating these to subpackage pin density.

With the information provided, one can make projections of preferred wiring images and their probable costs in terms of expected overflows. The data given here extend the analytical and experimental work done earlier on wiring track capacity alone [9]. Perhaps the most significant remaining variable left unevaluated is the relationship of package and subpackage input/output connector disposition and numbers to wireability of the package. The basic need here is for a workable approach to hierarchical and iterative placement, pin assignment, and wiring programs operating at all the package levels. This would have to permit electrical and timing constraints also to have their effect. It is clear that these are not small tasks.

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